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June 4, 2007

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Appl. No.	: 10/811,107	Confirmation No. 9214
Applicant	: Hironobu FUKUI	
Filed	: March 26, 2004	
TC/A.U.	: 2822	
Examiner	: Monica LEWIS	
Atty Docket No.	: 351991-992050 (previously 2102475-992050)	
Customer No.	: 26379	

Title: METAL OXIDE SEMICONDUCTOR (MOS) TYPE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

AMENDMENT AND RESPONSE TO OFFICE ACTION

M/S: AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Office Action of May 3, 2007, please enter the amendments set forth below and consider the following remarks.

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (**original**): A semiconductor device having a metal oxide semiconductor (MOS) type transistor structure, comprising:

an additional load capacitance that is formed at a part of the semiconductor device, which is vulnerable to soft errors.

2. (**original**): The semiconductor device according to claim 1, wherein the part that is vulnerable to soft errors is a first diffusion layer region, and the first diffusion layer region is at least a part of diffusion layer regions formed in the MOS type transistor structure and is connected to neither a power supply nor a ground.

3. (**original**): The semiconductor device according to claim 1, wherein the formation of the additional load capacitance is performed such that a well region that is formed immediately below the first diffusion layer region is made to have a higher concentration than other well region.

4. (**original**): The semiconductor device according to claim 3, wherein an impurity concentration at a junction interface between the well region with the higher concentration and the first diffusion layer region is set at 5×10^{18} to $10^{19}/cm^3$, and an impurity concentration at a junction interface between the other well region and a second diffusion layer region which is the diffusion layer regions except for the first diffusion layer region is set at $10^{18}/cm^3$.

5. (**withdrawn**): The semiconductor device according to claim 1, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS type transistor.

6. (**withdrawn**): The semiconductor device according to claim 5, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SRAM) type memory cell having a flip-flop circuit that comprises a plurality of the n-type MOS transistors and a plurality of p-type MOS transistors.

7. (**withdrawn**): The semiconductor device according to claim 1, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor and a p-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS transistor and a drain of the p-type MOS transistor.

8. (**withdrawn**): The semiconductor device according to claim 7, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SPAM) type memory cell having a flip-flop circuit that comprises a plurality of the n-type MOS transistors and a plurality of the p-type MOS transistors.

9. (**withdrawn**): A semiconductor device having a metal oxide semiconductor (MOS) type transistor structure, comprising:

a buried well region that is formed at a part of the semiconductor device, which is vulnerable to soft errors.

10. (**withdrawn**): The semiconductor device according to claim 9, wherein the part that is vulnerable to soft errors is a first diffusion layer region, and the first diffusion layer region is at least a part of diffusion layer regions formed in the MOS type transistor structure and is connected to neither a power supply nor a ground.

11. (**withdrawn**): The semiconductor device according to claim 9, wherein the formation of the buried well region is performed such that a well region that is formed immediately below the first diffusion layer region is made to have a triple-well structure.

12. (**withdrawn**): The semiconductor device according to claim 11, wherein the well region that is formed immediately below the first diffusion layer region, where the buried well region is formed, is made to have a triple-well structure, and other well region is

made to have a twin-well structure.

13. (**withdrawn**): The semiconductor device according to claim 9, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS type transistor.

14. (**withdrawn**): The semiconductor device according to claim 13, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SRAM) type memory cell having a flip-flop circuit that comprises a plurality of the n-type MOS transistors and a plurality of p-type MOS transistors.

15. (**withdrawn**): The semiconductor device according to claim 9, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor and a p-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS transistor and a drain of the p-type MOS transistor.

16. (**withdrawn**): The semiconductor device according to claim 15, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SRAM) type memory cell having a flip-flop circuit that comprises a plurality of said n-type MOS transistors and a plurality of said p-type MOS transistors.

17. (**withdrawn**): A method of manufacturing a semiconductor device having a metal oxide semiconductor (MOS) type transistor structure, comprising:

specifying by circuit simulation a part of the semiconductor device, which is vulnerable to soft errors; and

forming an additional load capacitance at the part of the semiconductor device, which is vulnerable to soft errors.

18. (**withdrawn**): The method of manufacturing a semiconductor device, according to

claim 17, wherein the formation of the additional load capacitance is performed such that additional ion implantation is selectively performed in addition to ordinary ion implantation at a time of forming a well region in the MOS type transistor structure, whereby a well region having a higher concentration than the other well region is formed at the part that is vulnerable to soft errors.

19. (**withdrawn**): A method of manufacturing a semiconductor device having a metal oxide semiconductor (MOS) type transistor structure, comprising:

specifying by circuit simulation a part of the semiconductor device, which is vulnerable to soft errors; and

forming a buried well region at the part of the semiconductor device, which is vulnerable to soft errors.

20. (**withdrawn**): The method of manufacturing a semiconductor device, according to claim 19, wherein the formation of the buried well region is performed such that the well region of the part that is vulnerable to soft errors is made to have a triple-well structure, and the other well region is made to have a twin-well structure.

REMARKS

Prior to this response, claims 1-20 were pending, with claims 17-20 previously withdrawn. In the Office Action of May 3, 2007, the Examiner issued a restriction/election requirement between "Embodiment I (Claims 1-4)," "Embodiment II (Claims 1 and 5)," "Embodiment III (Claims 1 and 6)," "Embodiment IV (Claims 1 and 7)," "Embodiment V (Claims 1 and 8)," "Embodiment VI (Claims 9-12)," "Embodiment VII (Claims 9 and 13)," "Embodiment VIII (Claims 9, 14 and 16)," and "Embodiment IX (Claims 9 and 15)."

In response to the requirement, Applicants hereby elect "Embodiment I (claims 1-4)." In the interests of expediting prosecution and avoiding additional costs, this election is made without traverse, as well as without acquiescence, surrender or disclaimer relating to any aspects contrary to Applicants' interests.

Claims 5-16 have been withdrawn from consideration.

It is respectfully noted that, upon allowance of a generic claim, Applicants are entitled to consideration/rejoinder of claims to additional (non-elected) species, which will also ordinarily be allowable. *See, e.g.,* 37 C.F.R. §1.141(a) and MPEP §806.04(d).

The Examiner is invited to call Applicant's attorney at the number below if doing so will facilitate prosecution of this application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit in the overpayment, to Deposit Account No. **07-1896** referencing Attorney Docket No. **351991-992050.**

Respectfully submitted,

DLA PIPER U.S. LLP

Dated: June 4, 2007

By: _____

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